Dr.-Ing. Jan Moritz Joseph

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Education

2014 – 2019	**Dr.-Ing. (PhD): "Networks-on-Chip for heterogeneous 3D System-on-Chips"**, graduation grade: summa cum laude (with highest honors). *Otto-von-Guericke-Universität Magdeburg*, Germany.
2011 – 2014	**M. Sc. Computer Science**, graduation grade: 1.4. Thesis topic: "A Dynamical Model of Scientific Collaboration Networks", thesis grade: 1.0, *Universität zu Lübeck*, Germany.
2008 – 2011	**B. Sc. Medical Engineering Sciences**, graduation grade: 1.5. Thesis topic: "Clusteranalysis in Molecular Dynamic Simulations", thesis grade" 1.0, *Universität zu Lübeck*.
2000 – 2008	**High school**, graduation grade 1.3 (3rd best grade in school) *Thomas-Mann-Schule*, Lübeck, Germany.

Work Experience

Since 06/2020	**Postdoctoral Researcher**, *RWTH Aachen University*, Germany.
09/2019 – 02/2020	**Visiting Researcher**, *Georgia Institute of Technology*, Atlanta, GA. • Heterogeneous 3D integration for DNN accelerators (systolic arrays).
04/2014 – 08/2019	**Research Assistant**, *Technische Universität Hamburg, Universität zu Lübeck and Otto-von-Guericke-Universität Magdeburg*, Germany (relocated with supervisor). • DFG projects "Detection and adaptive prioritization of semi-static data streams in Network-on-Chips" and "Technology-aware Asymmetric 3D-Interconnect Architectures: Templates and Design Methods". • 13 peer-reviewed publications as first author (three high-ranking journals).
04/2014 – 08/2019	**Managing Partner and Consultant**, *Systemische Potentiale Consulting GbR, Munich*. • Development of tool to measure organizational change, employee surveys and 360° feedbacks, e.g., for Sunny Cars GmbH.
2013 – 2014	**Student Assistant**, *Deutsche Physikalische Gesellschaft*, Bonn, Germany.
2009 – 2013	**Tutor**: mathematics, experimental and theoretical physics, *Universität zu Lübeck*.

Awards and Scholarships

2020	**Award** for best PhD thesis of the faculty 2020, Fakultät für Elektro- und Informationstechnik, Otto-von-Guericke Universität Magdeburg, Germany.
09/2019 – 02/2020	**Fellow** of German Academic Exchange Service (DAAD), stay at Georgia Tech, IFI Program.
2008 – 2014	**Scholar** of German merit foundation (Studienstiftung des deutschen Volkes).
2003	**Award** "Förderpreis des Geschichtswettbewerbs des Bundespräsidenten".

Skills

Courses

2019	Comprehensive Digital IC Implementation and Sign-Off (with Cadence), Rutherford Appleton Labs, Oxfordshire, UK.

Languages

	German: mother tongue. English: fluent. Latin: advanced. Frensh, Arabic: basic.
03/2011	English language course, *Hilderstone College*, Broadstairs, England.
08/2012	Arabic language course, *Landesspracheninstitut*, Bochum, Germany.

Voluntary Work

Since 2016	Member of commission for scholar selection, *German merit foundation*.
Since 2020	Elected treasurer of the regional chapter Leipzig, Halle, Magdeburg of the alumni of the *German merit foundation (Alumni der Studienstiftung e.V.)*.

2017 – 2020	Elected president of the regional chapter in Magdeburg of the alumni of the *German merit foundation (Alumni der Studienstiftung e.V.)*: Organization of trans-regional scientific talks ”Hemisphärenkolloquium” (speakers from universities, Fraunhofer- and Max-Planck-Gesell.).
07/2016	Professional training in scholarship holder selection (”Beobachterschulung”).
2012 – 2013	Elected manager of the IT department of the General Students' Committee.
2011 – 2013	Elected speaker of scholars in Lübeck: Organization of events and meetings.

Peer-reviewed Articles in Journals

[1] **Jan Moritz Joseph**, Dominik Ermel, Lennart Bamberg, Alberto García-Oritz, and Thilo Pionteck. “Application-Specific SoC Design Using Core Mapping to 3D Mesh NoCs with Nonlinear Area Optimization and Simulated Annealing”. In: *Technologies* 8.1 (2020), p. 10. DOI: 10.3390/technologies8010010.

[2] Lennart Bamberg, **Jan Moritz Joseph**, Thilo Pionteck, and Alberto Garcia-Ortiz. “Cross-talk optimization for through-silicon vias by exploiting temporal signal misalignment”. In: *Integration* 67 (2019), pp. 60–72. DOI: 10.1016/j.vlsi.2019.04.009.
Impact Factor: 1.105 (JCR 2018).

[3] **Jan Moritz Joseph**, Lennart Bamberg, Dominik Ermel, Behnam Razi Perjikolaei, Anna Drewes, Alberto García-Ortiz, and Thilo Pionteck. “NoCs in Heterogeneous 3D SoCs: Co-Design of Routing Strategies and Microarchitectures”. In: *IEEE Access* 7 (2019), pp. 135145–135163. DOI: 10.1109/ACCESS.2019.2942129.
Impact Factor: 4.098 (JCR 2018).

[4] **Jan Moritz Joseph**, Lennart Bamberg, Imad Hajjar, Robert Schmidt, Thilo Pionteck, and Alberto Garcia-Ortiz. “Simulation environment for link energy estimation in networks-on-chip with virtual channels”. In: *Integration* 68 (2019), pp. 147–156. DOI: 10.1016/j.vlsi.2019.05.005.
Impact Factor: 1.105 (JCR 2018).

[5] **Jan Moritz Joseph**, Christopher Blochwitz, Alberto García-Ortiz, and Thilo Pionteck. “Area and power savings via asymmetric organization of buffers in 3D-NoCs for heterogeneous 3D-SoCs”. In: *Microprocessors and Microsystems* 48 (2017), pp. 36–47. DOI: 10.1016/j.micpro.2016.09.011.
Impact Factor: 1.045 (JCR 2018).

Peer-reviewed Articles in Proceedings

[6] **Jan Moritz Joseph**, Lennart Bamberg, Jeong Geonhwa, Ruei-Ting Chien, Rainer Leupers, Alberto García-Oritz, Tushar Krishna, and Thilo Pionteck. “Bridging the Frequency Gap in Heterogeneous 3D SoCs through Technology-Specific NoC Router Architectures”. In: *26th Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE. 2021. *24% acceptance rate*.

[7] **Jan Moritz Joseph**, Anand Samajdar, Lingjun Zhu, Rainer Leupers, Syun-Kun Lim, Thilo Pionteck, and Tushar Krishna. “Bridging the Frequency Gap in Heterogeneous 3D SoCs through Technology-Specific NoC Router Architectures”. In: *22nd International Symposium on Quality Electronic Design (ISQED)*. IEEE. 2021. *accepted, unpublished*.

[8] Anna Drewes, **Jan Moritz Joseph**, Bala Gurumurthy, David Broneske, Gunter Saake, and Thilo Pionteck. “Optimising Operator Sets for Analytical Database Processing on FPGAs”. In: *International Symposium on Applied Reconfigurable Computing*. Springer. 2020, pp. 30–44. DOI: 10.1007/978-3-030-44534-8_3.

[9] Anand Samajdar, **Jan Moritz Joseph**, Yuhao Zhu, Paul Whatmough, Matthew Mattina, and Tushar Krishna. “A Systematic Methodology for Characterizing Scalability of DNN Accelerators”. In: *International Symposium on Performance Analysis of Systems and Software (ISPASS)*. IEEE. 2020.

[10] Daniele Passaretti, **Jan Moritz Joseph**, and Thilo Pionteck. “Survey on FPGAs in Medical Radiology Applications: Challenges, Architectures and Programming Models”. In: *2019 International Conference on Field-Programmable Technology (ICFPT)*. IEEE. 2019, pp. 279–282. DOI: 10.1109/ICFPT47387.2019.00047.

[11] **Jan Moritz Joseph**, Dominik Ermel, Lennart Bamberg, Alberto García Oritz, and Thilo Pionteck. “System-Level Optimization of Network-on-Chips for heterogeneous 3D System-on-Chips”. In: *2019 IEEE 37th International Conference on Computer Design (ICCD)*. IEEE. 2019, pp. 409–412. DOI: 10.1109/ICCD46524.2019.00064.

[12] **Jan Moritz Joseph**, Dominik Ermel, Tobias Drewes, Lennart Bamberg, Alberto García-Oritz, and Thilo Pionteck. “Area Optimization with Non-linear Models in Core Mapping for System-on-Chips”. In: *2019 8th International Conference on Modern Circuits and Systems Technologies (MOCAST)*. IEEE. 2019, pp. 1–4. DOI: 10.1109/MOCAST.2019.8742035.

[13] Lennart Bamberg, **Jan Moritz Joseph**, Robert Schmidt, Thilo Pionteck, and Alberto García-Ortiz. “Coding-aware Link Energy Estimation for 2D and 3D Networks-on-Chip with Virtual Channels”. In: *2018 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*. IEEE. 2018, pp. 222–228. DOI: 10.1109/PATMOS.2018.8464171.

[14] Christopher Blochwitz, Julian Wolff, Mladen Berekovic, Dennis Heinrich, Sven Groppe, **Jan Moritz Joseph**, and Thilo Pionteck. “Hardware-Accelerated Index Construction for Semantic Web”. In: *2018 International Conference on Field-Programmable Technology (FPT)*. IEEE. 2018, pp. 278–281. DOI: 10.1109/FPT.2018.00053.

[15] Tobias Drewes, **Jan Moritz Joseph**, Bala Gurumurthy, David Broneske, Gunter Saake, and Thilo Pionteck. “Efficient Inter-Kernel Communication for OpenCL Database Operators on FPGAs”. In: *2018 International Conference on Field-Programmable Technology (FPT)*. IEEE. 2018, pp. 266–269. DOI: 10.1109/FPT.2018.00050.

[16] **Jan Moritz Joseph**, Lennart Bamberg, Gerald Krell, Imad Hajjar, Alberto Garcia-Oritz, and Thilo Pionteck. “Specification of Simulation Models for NoCs in Heterogeneous 3D SoCs”. In: *2018 13th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. IEEE. 2018, pp. 1–8. DOI: 10.1109/ReCoSoC.2018.8449387.

[17] Christopher Blochwitz, Raphael Klink, **Jan Moritz Joseph**, and Thilo Pionteck. “Continuous live-tracing as debugging approach on FPGAs”. In: *2017 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. IEEE. 2017, pp. 1–8. DOI: 10.1109/RECONFIG.2017.8279783.

[18] Christopher Blochwitz, Julian Wolff, **Jan Moritz Joseph**, Stefan Werner, Dennis Heinrich, Sven Groppe, and Thilo Pionteck. “Hardware-accelerated radix-tree based string sorting for Big data applications”. In: *International Conference on Architecture of Computing Systems*. Springer, Cham. 2017, pp. 47–58. DOI: 10.1007/978-3-319-54999-6_4.

[19] Tobias Drewes, **Jan Moritz Joseph**, and Thilo Pionteck. “An FPGA-based prototyping framework for Networks-on-Chip”. In: *2017 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. IEEE. 2017, pp. 1–7. DOI: 10.1109/RECONFIG.2017.8279775.

[20] **Jan Moritz Joseph**, Lennart Bamberg, Sven Wrieden, Dominik Ermel, Alberto Garcia-Oritz, and Thilo Pionteck. “Design method for asymmetric 3D interconnect architectures with high level models”. In: *2017 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. IEEE. 2017, pp. 1–8. DOI: 10.1109/ReCoSoC.2017.8016143.

[21] **Jan Moritz Joseph**, Morten Mey, Kristian Ehlers, Christopher Blochwitz, Tobias Winker, and Thilo Pionteck. “Design space exploration for a hardware-accelerated embedded real-time pose estimation using Vivado HLS”. In: *2017 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. IEEE. 2017, pp. 1–8. DOI: 10.1109/RECONFIG.2017.8279785.

[22] **Jan Moritz Joseph**, Chritopher Blochwitz, and Thilo Pionteck. “Adaptive allocation of default router paths in Network-on-Chips for latency reduction”. In: *2016 International Conference on High Performance Computing & Simulation (HPCS)*. IEEE. 2016, pp. 140–147. DOI: 10.1109/HPCSim.2016.7568328.

[23] **Jan Moritz Joseph**, Tobias Winker, Kristian Ehlers, Christopher Blochwitz, and Thilo Pionteck. “Hardware-accelerated pose estimation for embedded systems using Vivado HLS”. In: *2016 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. IEEE. 2016, pp. 1–7. DOI: 10.1109/ReConFig.2016.7857173.

[24] **Jan Moritz Joseph**, Sven Wrieden, Christopher Blochwitz, Alberto García-Oritz, and Thilo Pionteck. “A simulation environment for design space exploration for asymmetric 3D-Network-on-Chip”. In: *2016 11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC)*. IEEE. 2016, pp. 1–8. DOI: 10.1109/ReCoSoC.2016.7533908.

[25] Christopher Blochwitz, **Jan Moritz Joseph**, Rico Backasch, Thilo Pionteck, Stefan Werner, Dennis Heinrich, and Sven Groppe. “An optimized radix-tree for hardware-accelerated dictionary generation for semantic web databases”. In: *2015 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*. IEEE. 2015, pp. 1–7. DOI: 10.1109/ReConFig.2015.7393291.

[26] **Jan Moritz Joseph**, Christopher Blochwitz, Thilo Pionteck, and Alberto García-Ortiz. “Area and power savings via buffer reorganization in asymmetric 3D-NoCs for heterogeneous 3D-SoCs”. In: *2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC)*. IEEE. 2015, pp. 1–4. DOI: 10.1109/NORCHIP.2015.7364370.

[27] **Jan Moritz Joseph** and Thilo Pionteck. “A cycle-accurate network-on-chip simulator with support for abstract task graph modeling”. In: *2014 International Symposium on System-on-Chip (SoC)*. IEEE. 2014, pp. 1–6. DOI: 10.1109/ISSOC.2014.6972440.

Further Publications

2020 **DATE 2020 PhD Forum**: Presentation of PhD thesis.

2019 **Jan Moritz Joseph:** ”Networks-on-Chip for heterogeneous 3D Systems-on-Chip”, Otto-von-Guericke-Universität Magdeburg, Fakultät für Elektrotechnik und Informationstechnik, DOI: 10.25673/14125

Funding

2019 **DAAD (German Academic Exchange Service) Fellowship** for stay at Georgia Institute of Technology, IFI Program (Internationale Forschungsaufenthalte für Informatiker - Doktoranden), **12,000 €**

Projects

Ratatoskr: An open-source design and simulation framework for NoCs in heterogeneous 3D SoCs github.com/jmjos/ratatoskr

Professional Activities

Technical Committee Activities

Committee Member & Technical Reviewer; 14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2020)

Committee Member & Technical Reviewer; 22nd IEEE International Symposium on Quality Electronic Design (ISQED 2021)

Conference Activities

Virtual / Local Arrangement Chair; 14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2020)

Technical Reviewer

External Reviewer for *DAC 2020*
Reviewer for *IEEE Access*
Reviewer for *IEEE Transactions on Industrial Electronics*
Reviewer for *Integrations, the VLSI journal*

Other Activities and Interests

25 years of playing the piano; special interest in composition and improvisation (Jazz and Blues)
12 years of active memberships in golf and dance clubs

Reference Persons

Prof. Rainer Leupers
RWTH Aachen University, Germany
Head of Institute for Communication Technologies and Embedded Systems

Prof. Tushar Krishna
Georgia Institute of Technology, Atlanta, GA
Assistant Professor; ON Semiconductor Junior Professor

Prof. Dr.-Ing. Thilo Pionteck
Otto-von-Guericke Univeristät Magdeburg, Germany
Head of Institute for Information Technology and Communications

Prof. Dr.-Ing. Alberto García-Oritz
Universität Bremen, Germany
Chair for Integrated Digital Systems, ITEM